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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,151	02/26/2004	Mitsutoshi Miyasaka	118490	7277

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,151	MIYASAKA, MITSUTOSHI	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/28/06 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3 and 5-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (US 2003/0092213 A1).

In re claim 1, Yamazaki discloses a complementary transistor circuit, comprising:

a first transistor; and

a second transistor that has a conductivity type that is different from a conductivity type of the first transistor (CMOS; column 11, lines 34-36),

the first transistor having a first channel region formed in one single crystal grain (column 16, l ines 26-28), and

the second transistor having a second channel region formed in the one single crystal grain (column 16, lines 26-28)[1].

In re claim 3, Yamazaki discloses the device of claim 1, further comprising:

a first electric field relief region (119) which is formed at both sides of the first channel region; and

a second electric field relief region (119) which is formed at both sides of the second channel region,

the first electric field relief region and the second electric field relief region are composed of low-concentration impurity regions, and

the first electric field relief region and the second electric field relief region formed in the one single crystal rain.

In re claim 5, Yamazaki discloses the device of claim 1, the first transistor and the second transistor are formed in a semiconductor film in which the one single crystal grain is patterned in a U shape (as can be seen in Figs. 12A – 12C, comprising a U-shape between each channel region).

In re claim 6, Yamazaki discloses the complementary transistor circuit according to claim 1, the first transistor and the second transistor formed in a semiconductor film in

[1] also (column 7, lines 10-11; column 9, lines 12-16).

which the one single crystal grain is patterned in a rectangular shape (as seen in Figs. 12A – 12C, the channel region itself is rectangular shaped).

In re claim 7, Yamazaki discloses the complementary transistor circuit according to claim 1. The limitation, "... formed by carrying out a heat treatment on an amorphous or a polycrystalline semiconductor film" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. Therefore, in terms of a device limitation, to which these claims are drawn, this limitation is not given any patentable weight.

In re claim 8, Yamazaki discloses the complementary transistor circuit according to claim 7, the one single crystal grain is formed substantially centered on a starting-point portion that is a concave portion formed on an insulating substrate (as seen in Figs. 12A – 12C).

In re claims 9-11, Yamazaki disclose the complementary transistor circuit according to claim 8. The limitations including, "the one single crystal grain is formed by carrying out the heat treatment on the semiconductor film ... melted" and "... laser irradiation" refer to the process for making this product and does not further distinguish the claimed structure over the prior art. Therefore, in terms of a device limitation, to which these claims are drawn, this limitation is not given any patentable weight.

In re claim 12, Yamazaki discloses an electro-optical device, comprising: the complementary transistor circuit according to claim 1.

In re claim 13, Yamazaki discloses an electronic apparatus comprising: the complementary transistor circuit according to claim 1.

In re claim 14, Yamazaki discloses a complementary thin film transistor circuit, comprising:

a first-conductive type thin film transistor and a second-conductivity-type thin film transistor formed using same-single crystal grain (column 16, lines 26-28), the single crystal

grain being formed substantially centered on a pre-positioned starting-point portion disposed on an insulating surface of a substrate.

In re claim 15, Yamazaki discloses the complementary thin film transistor circuit according to claim 14, further comprising: electric field relief regions (119) which are formed at both sides of channel regions of the first-conductive type thin film transistor and the second-conductivity-type type thin film transistor, the channel regions being sandwiched between the electric field relief regions, which are composed of low-concentration impurity regions, the electric field relief regions and the channel regions formed in the same single crystal grain.

In re claim 16, Yamazaki discloses the complementary thin film transistor circuit according to claim 14, further comprising channel regions formed in a region in the single crystal grain that does not include the staring-point portion.

In re claim 17, Yamazaki discloses the complementary thin film transistor circuit according to claim 16, the first-conductive type thin film transistor and the second-conductive type thin film transistor formed in a semiconductor film in which the single crystal grain is patterned in a U shape (as can be seen in Figs. 12A – 12C, the U-shaped single crystal between the channel regions).

In re claim 18, Yamazaki discloses the complementary thin film transistor circuit according to claim 16, the first- conductive type thin film transistor and the second-conductive type thin film transistor formed in a semiconductor film in which the single crystal grain is patterned in a rectangular shape (the channel region itself is rectangular shaped).

In re claim 19, Yamazaki discloses the complementary thin film transistor circuit according to claim 14. The limitation, "the single crystal grain formed by carrying out a heat treatment on an amorphous or a polycrystalline semiconductor film" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. Therefore, in terms of a device limitation, to which these claims are drawn, this limitation is not given any patentable weight.

In re claim 20, Yamazaki discloses the complementary thin film transistor circuit according to claim 19, the starting-point portion being a concave portion formed on an insulation substrate.

In re claim 21, Yamazaki discloses the complementary transistor circuit according to claim 1, the first transistor and the second transistor being formed on an insulating film.

In re claim 22, Yamazaki discloses the complementary transistor circuit according to claim 21, the first channel region and the second channel region not overlapping a concave portion formed in the insulating film.

In re claim 23, Yamazaki discloses a semiconductor device, comprising:
a plurality of complementary transistor circuits accordingly to claim 1.

Response to Arguments

Applicant's arguments with respect to claims 1, 3 and 5-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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